Page 14, line 5, replace "FIGs. 15A, 15B and 15C" with --FIGs. 15A, 15B, 15C and 15D--.

Page 14 line 17, replace "FIG. 18 is" with --FIGs. 18A and 18B, arranged as shown in FIG. 18, are--.

Page 15, line 12, replace "FIGs. 24A and 24B" with --FIGs. 24A, 24B and 24C--.

Page 109, lines 1-2, delete the title of the abstract and substitute therefore --Memory Controller for Controlling Memory Accesses Across Networks in Distributed Shared Memory Processing Systems--.

A4

IN THE CLAIMS

Cancel claims 2-30.

Amend claim 1, as follows:

1. [Amended] A cache coherency system for a shared memory parallel processing system including a plurality of processing nodes, comprising: a multi-stage communication network for interconnecting said processing nodes; each said processing node including one or more caches for storing a plurality of cache lines; and a cache coherency directory which is distributed to each of said nodes for tracking which of said nodes have copies of each cache line.

Add new claims 31-39, as follows:

31. A method for operating a shared memory parallel processing system as a cache coherency system including a plurality of processing nodes, comprising the steps of:

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches;

distributing to each of said processing nodes a cache

coherency directory; and

tracking in said cache coherency directory which of said processing nodes have copies of each cache line.

32. A program storage device readable by a machine, tangibly embodying a program of instructions executable by a machine to perform method steps for operating a shared memory parallel processing system including a plurality of processing nodes, said method steps comprising:

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches; and

tracking in a cache coherency directory which is distributed to each of said processing nodes which of said processing nodes have copies of each cache line.

33. An article of manufacture comprising:

a computer useable medium having computer readable program code means embodied therein for operating a shared memory parallel processing system including a plurality of processing nodes, the computer readable program means in said article of manufacture comprising:

computer readable program code means for causing a computer to effect interconnecting said processing nodes through a multi-stage communication network;

computer readable program code means for causing a computer to effect storing at each said processing node a plurality of cache lines in one or more caches; and

computer readable program code means for causing a computer to effect tracking in a cache coherency directory which is distributed to each of said processing nodes which of said processing nodes have copies of each cache line.

34. A computer program product or computer program element for operating a shared memory parallel processing system including a plurality of processing nodes according to the steps of:

interconnecting said processing nodes through a multi-stage communication network;

storing at each said processing node a plurality of cache lines in one or more caches;

distributing to each of said processing nodes a cache coherency directory; and

tracking in said cache coherency directory which of said processing nodes have copies of each cache line.

35. The cache coherency system of claim 1, further comprising:

a shared memory including a first memory portion for storing unchangeable data and a second memory portion for storing changeable data; and

said cache coherency directory listing which nodes of said plurality of processing nodes have accessed copies of said cache lines in said second memory portion.

36. The cache coherency system of claim 35, each of said plurality of processing nodes being operable for reading, storing, and invalidating said shared memory at any other of said processing nodes.

37. The cache coherency system of claim 36, further comprising at a first node of said plurality of processing nodes a memory controller selectively operable first responsive to a request for access to a memory word for first accessing the cache at said first node and selectively operable second responsive to being unable to access said memory word in said cache at said first node for accessing said memory word selectively from a cache line in said memory or from a remote memory and storing said cache line to said cache at said first node.